	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	2	6667210.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 13:35	
2	BRS	L2	120	schneider near paul.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 13:37	
3	BRS	L3	1598	438/257.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 13:38	
4	BRS	L5	29	3 and inter near polysilicon	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 13:38	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L4	23	3 and inter-polysilicon	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:02	
6	BRS	L6	17	3 and ipd	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:03	
7	BRS	L7	1642	inter-polysilicon or inter near polysilicon or ipd	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:04	
8	BRS	L8	54	(inter-polysilicon or inter near polysilicon or ipd) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:05	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	54	((inter-polysilicon) or (inter near polysilicon) or (ipd)) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:15	
10	BRS	L10	7	((inter-polysilicon) or (inter near polysilicon) or (ipd)) near25 (hardmask or hard near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:24	
11	BRS	L11	331	remov$3 near5 hardmask	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:24	
12	BRS	L12	3	(remov$3 near5 hardmask) near25 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:25	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
13	BRS	L13	36	(remov$3 near5 hard near mask) near25 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:32	
14	BRS	L14	117	(pattern$3 near5 hard near mask) near25 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:41	
15	BRS	L15	157	(etch$3 near15 hard near mask) near25 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 14:58	
16	BRS	L16	20	(etch$3 near15 hardmask) near25 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:00	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
17	BRS	L17	2141	(etch$3 near15 mask) near35 (memory)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:01	
18	BRS	L18	402	(etch$3 near15 mask) near35 (memory) near35 (polysilicon)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:18	
19	BRS	L19	687	(etch$3 near15 mask) near35 (memory) near35 (remov$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:18	
20	BRS	L20	2	(etch$3 near15 hardmask) near35 (memory) near35 (remov$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:19	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
21	BRS	L21	40	(etch$3 near15 hard near mask) near35 (memory) near35 (remov$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/04/13 15:19	

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	☐	☐	US 20020127800 A1	Flash memory cell process using a hardmask	438/257	6	20020912
2	☐	☐	US 6667210 B2	Flash memory cell process using a hardmask	438/257	6	20031223
3	☐	☐	US 6239458 B1	Polysilicon-via structure for four transistor, triple polysilicon layer SRAM cell including two polysilicon layer load resistor	257/296	14	20010529
4	☐	☐	US 6214715 B1	Method for fabricating a self aligned contact which eliminates the key hole problem using a two step spacer deposition	438/597	15	20010410
5	☐	☐	US 6100138 A	Method to fabricate DRAM capacitor using damascene processes	438/253	25	20000808
6	☐	☐	US 5866449 A	Method of making polysilicon-via structure for four transistor, triple polysilicon layer SRAM cell including two polysilicon layer load resistor	438/238	13	19990202
7	☐	☐	TW 434884 A	Manufacturing method of bottom electrode of DRAM capacitor - is able to ease the alignment issue of photolithography		1	20010516